KX1400
Audio Playback IC

FEATURES

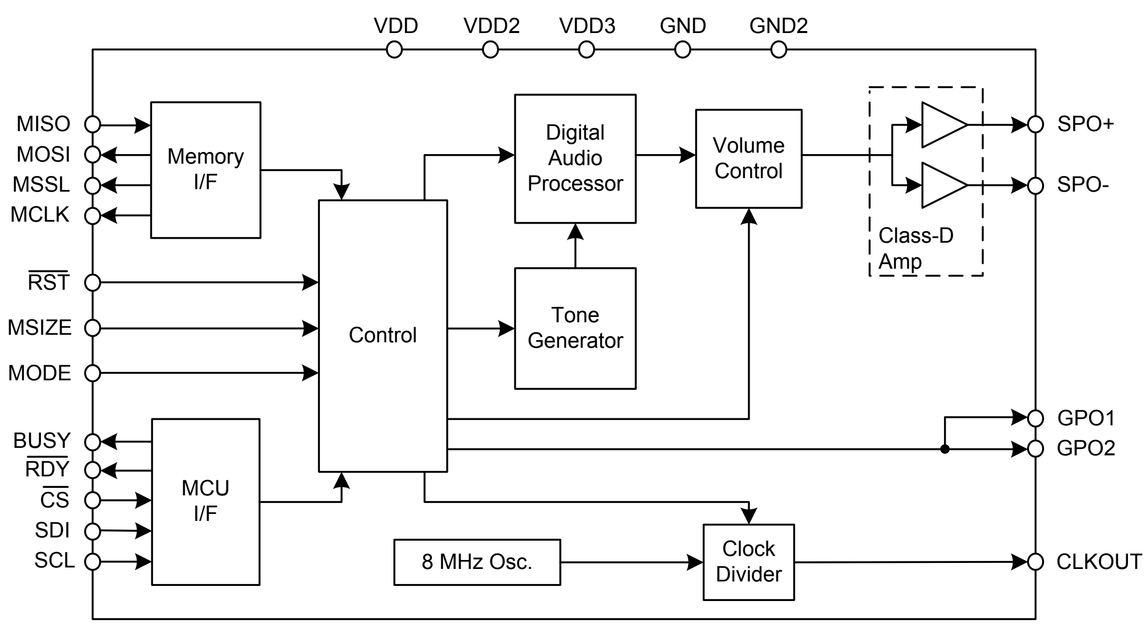
- Plays Pre-recorded 8kHz Audio Data
- On-chip Tone Generator
- Operates Stand-alone or as MCU Peripheral
- Built-in Digital Audio Processor
- Integrated Class-D Speaker Driver
- No External Low-pass Filter Required
- Digital Volume Control
- On-chip Oscillator – No XTAL Required
- Plays up to 4096 Pre-recorded Audio Phrases
- Configurable General-purpose Clock Output
- Two General-purpose Digital Outputs
- Low-power Standby State (1 μA Typ.)
- Operating Voltage: 2.7V – 5.5V
- Operating Temperature: -40°C to 85°C
- Packages:
  - 20-pin SOIC (KX1400EW)
  - 24-pin 4X4mm QFN (KX1400EG)

GENERAL DESCRIPTION

The KX1400 is an audio playback IC designed to play 8kHz audio data directly to an external speaker via an on-chip digital audio processor and Class-D driver. Both 12-bit PCM and 4-bit IMA ADPCM data formats are supported. It also has a built-in tone generator capable of generating tones at 4096 different frequencies. The on-chip audio processor alleviates the need for an external low-pass filter in most cases. The KX1400 utilizes low power CMOS technology and provides a stand-by power-savings state, making it well suited for battery powered applications.

The KX1400 operates in either a stand-alone mode or interfaced to a microcontroller (MCU) host. Audio data is provided to the KX1400 from either a user-programmed external serial memory or from the host MCU. Under MCU control, the user can select phrases or tone sequences to play from the external memory, play tone sequences via commands, or stream audio data directly to the on-chip audio processor. In stand-alone mode no MCU is required; on reset, the KX1400 plays a single phrase from external memory and then returns to a stand-by power-saving state.

FUNCTIONAL BLOCK DIAGRAM

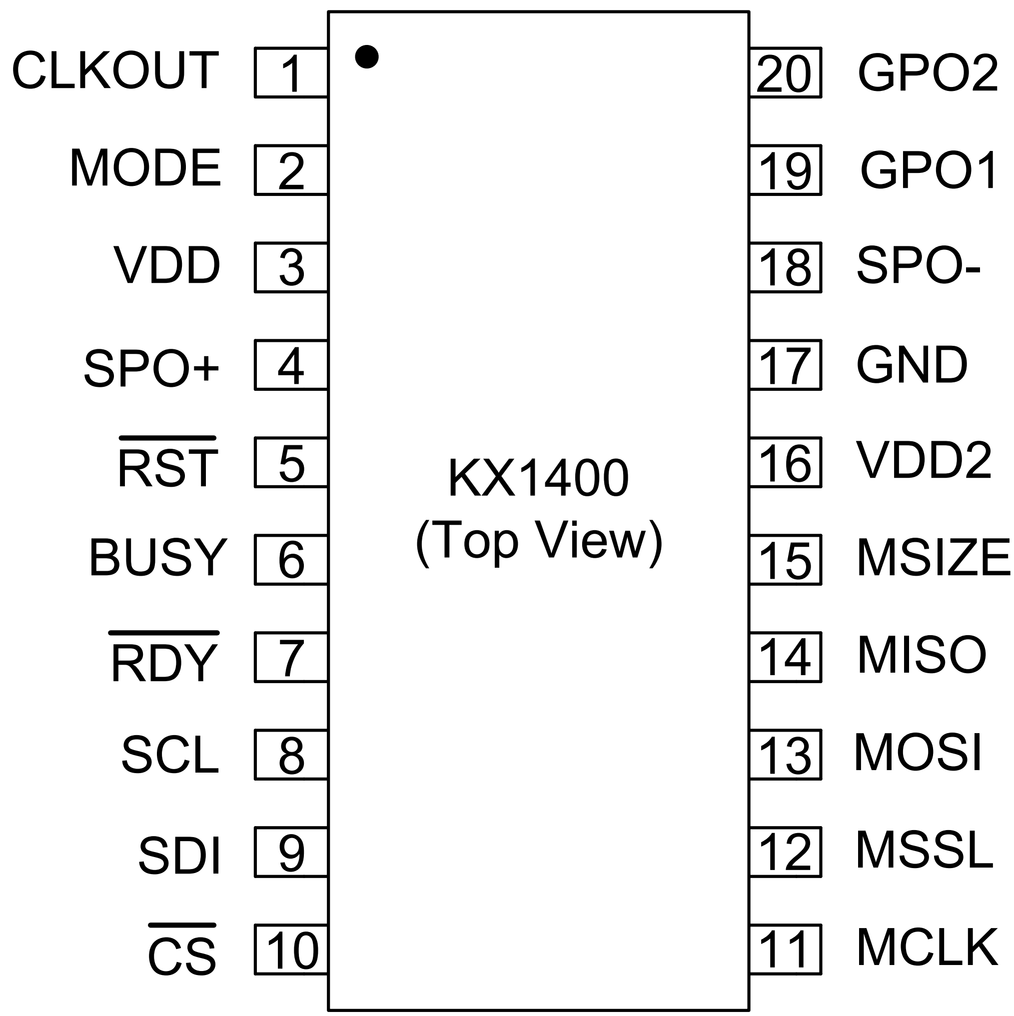


1. PIN DESCRIPTION AND PINOUT

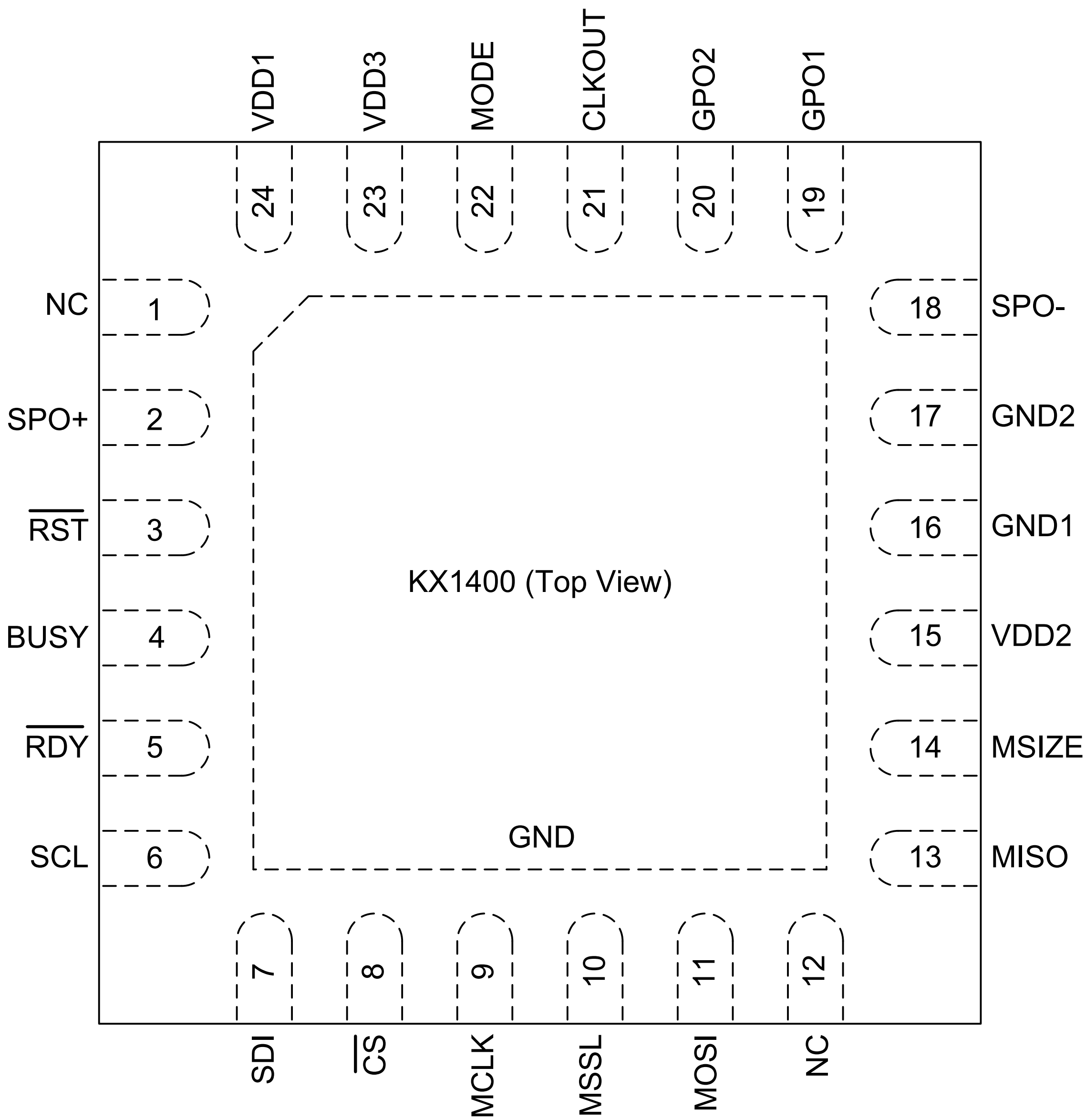
1.1. Pin Description

NAME	PIN NUMBER		TYPE	DESCRIPTION
	SOIC20	QFN24		
CLKOUT	1	21	Digital Output	General purpose clock output. Divided system clock.
MODE	2	22	Digital Input	Operation mode. Mode = 0, Stand-alone mode; Mode = 1, Host-controlled mode.
VDD1	3	23	Power	Supply voltage.
SPO+	4	2	Analog Output	Speaker output (+).
$\overline{RST}$	5	3	Digital Input	Reset. Active low input; resets the device when driven low. May be used as a start input when device is used in stand-alone mode.
BUSY	6	4	Digital Output	Host interface status: asserted by KX1400 when command execution is complete. Also used as MISO in SPI pass-thru mode.
$\overline{RDY}$	7	5	Digital Output	Host interface data request: asserted by KX1400 when ready to receive next command/data from host.
SCL	8	6	Digital Input	Host interface clock input.
SDI	9	7	Digital Input	Host interface serial data input.
$\overline{CS}$	10	8	Digital Input	Host interface chip select.
MCLK	11	9	Digital Output	Serial memory interface clock signal.
MSSL	12	10	Digital Output	Serial memory interface chip select.
MOSI	13	11	Digital Output	Serial memory interface data output.
MISO	14	13	Digital Input	Serial memory interface data input.
MSIZE	15	14	Digital Output	Memory address size: MSIZE = 0, memory uses 16-bit addresses; MSIZE = 1, memory uses 24-bit addresses.
VDD2	16	15	Power	Supply voltage.
GND1	17	16	Ground	Ground.
SPO-	18	18	Analog Output	Speaker output (-).
GPO1	19	19	Digital Output	General purpose digital output 1. Configured by host MCU.
GPO2	20	20	Digital Output	General purpose digital output 2. Configured by host MCU.
VDD3	-	24	Power	Supply voltage.
GND2	-	17	Ground	Ground.
NC	-	1	–	Not Connected.
NC	-	12	–	Not Connected.

1.2. KX1400EW 20-Lead SOIC Pin-out Diagram (Top View)

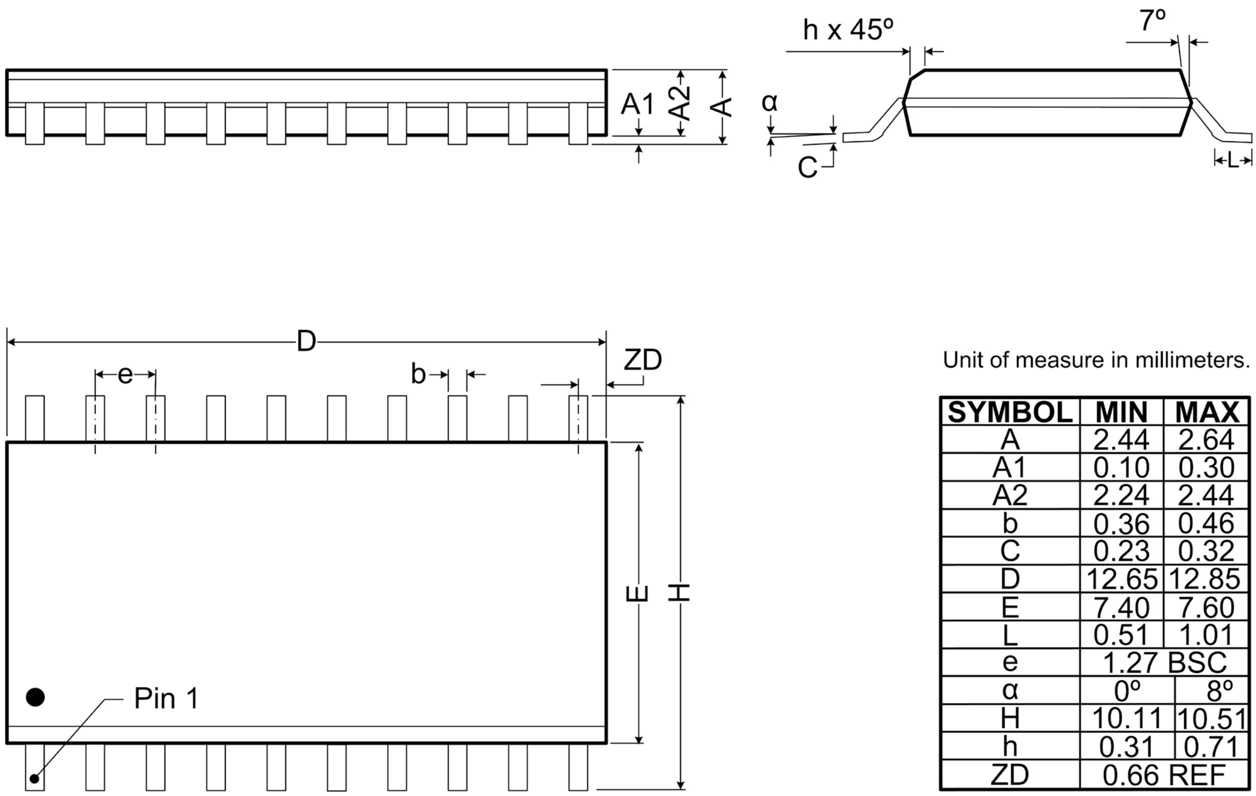


1.3. KX1400EG QFN-24 Pin-out Diagram (Top View)



2. PACKAGE DESCRIPTIONS

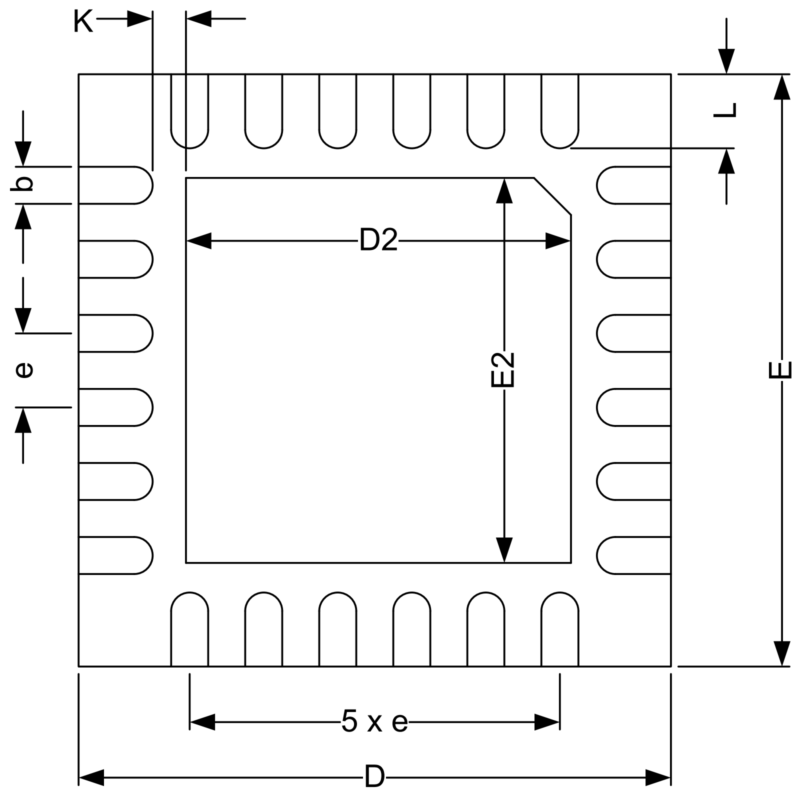
2.1. 20-Lead Wide Body SOIC Package Drawing (Package Type W)



Unit of measure in millimeters.

SYMBOL	MIN	MAX
A	2.44	2.64
A1	0.10	0.30
A2	2.24	2.44
b	0.36	0.46
C	0.23	0.32
D	12.65	12.85
E	7.40	7.60
L	0.51	1.01
e	1.27 BSC	
α	0º	8º
H	10.11	10.51
h	0.31	0.71
ZD	0.66 REF	

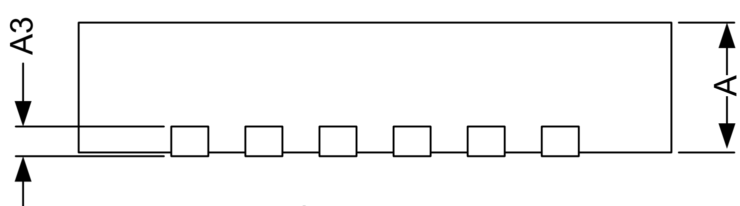
2.2. QFN-24 Package Drawing (Package Type G)



BOTTOM VIEW

A	0.90 TYP
A3	0.20 TYP
b	0.25 ± 0.05
K	0.20 min
D	4.00 ± 0.10
E	4.00 ± 0.10
e	0.50 TYP
D2	2.60 ± 0.10
E2	2.60 ± 0.10
L	0.30 ± 0.10

Unit of measure in millimeters.



SIDE VIEW

3. ABSOLUTE MAXIMUM RATINGS

Absolute Maximum Ratings are those values beyond which the life of the device may be impaired.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage (VDD)		-0.3		6.0	V
Voltage on Digital Input pins		-0.3		6.0	V
Current through VDD or GND				500	mA
Current through Digital Output Pins				200	mA
Current through SPO+ or SPO-				500	mA
Storage Temperature		-60		150	ºC
Lead Temperature	Soldering, 10 seconds			300	ºC

4. ELECTRICAL CHARACTERISTICS

Specifications are for T_A = -20°C to +70°C, VDD = 2.7V to 5.5V unless otherwise specified (Note1).

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VDD	Supply Voltage		2.7		5.5	V
IDD	Operating Supply Current	VDD = 3.3V, Muted		1.8		mA
		VDD = 3.3V, Playing Full-Volume 250Hz Tone into 16Ω Speaker		39		mA
		VDD = 3.3V, Playing Full-Volume 250Hz Tone into 8Ω Speaker		50		mA
VBO	Brown-out Voltage		1.6		2.4	V
ISB	Stand-by Current (Note 2)	VDD = 5.0V VDD = 3.3V		1.5 1.2		µA µA
VIH	Input High Voltage		0.7 * VDD			V
VIL	Input Low Voltage				0.3 * VDD	V
VOH	Output High Voltage	I_{OH} = -3mA I_{OH} = -10µA I_{OH} = -8mA	VDD-0.7 VDD-0.1 	 VDD-0.8		V
VOL	Output Low Voltage	I_{OL} = 8mA I_{OL} = 10µA I_{OL} = 25mA		 1.0	0.6 0.1 	V
CIN	Input Capacitive Load	Per Input		10		pF

Notes:

1. Specifications over the -20°C to +70°C operating range are assured by design, characterization, and correlation with statistical process controls.
2. Device placed in Stand-by state using Stand-by option of the Stop command (See Section 8.2)

5. OPERATING CHARACTERISTICS

Specifications are for T_A = -20°C to +70°C, VDD = 2.7V to 5.5V unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
fosc	Internal Oscillator Frequency	VDD = 3.3V, T = 25°C	8.07	8.192	8.32	MHz
Δf_{OSC}	Internal Oscillator Frequency Variation	2.7V ≤ VDD ≤ 3.6V	-1		+1	%
		2.7V ≤ VDD ≤ 5.5V	-1		+3	%
f_{SW}	Output Switching Frequency			256		kHz
THD	Total Harmonic Distortion	250Hz tone into 8Ω Load		40		dB
P_{OUT}	Maximum Output Power	VDD=3.3V, 8Ω Load		120		mW
		VDD=5V, 8Ω Load		320		mW
$\overline{RST}_{DELAY}$	Delay From $\overline{RST}$ High to Execution of First Command				20	µS
$\overline{RST}_{MIN}$	Minimum $\overline{RST}$ Low Time to Generate a System Reset		100			ns
$T_{CLKOUTH}$	Clock Out High Time	Fclkout = 8.2MHz	40		80	ns
$T_{CLKOUTL}$	Clock Out Low Time		40		80	ns

6. FUNCTIONAL DESCRIPTION

Using a fixed 8 KHz sample rate, the KX1400's audio processor decodes uncompressed 12-bit PCM or 4-bit IMA Adaptive Pulse Code Modulation (ADPCM) audio data and sends it to an on-chip, second-order noise shaping Digital Audio Processor (DAP). It can also generate audio data for 4096 different single-frequency tones. The DAP's output is connected to an on-chip class-D amplifier stage which provides differential outputs suitable for directly driving an external 8Ω speaker.

6.1. Operational Modes

The KX1400 supports two modes of operation: stand-alone mode and host-controlled mode. The mode of operation is determined by the state of the MODE pin as the KX1400 exits reset. Setting the MODE pin to a logic low state causes the KX1400 to operate in stand-alone mode. Setting MODE to logic high configures the KX1400 to operate in host-controlled mode.

6.1.1. Stand-alone Mode

In stand-alone mode, no host MCU is required. The KX1400 is connected directly to an external serial memory. On exit from a reset, the KX1400 processes the first phrase (command and data sequence) from external memory. In stand-alone mode, control of the KX1400 can be implemented as simply as relying on power-on-reset events or connecting a switch to the $\overline{RST}$ pin of the KX1400. Note: In stand-alone operation, the $\overline{CS}$ pin should be connected to VDD and the SCL and SDI pins connected to ground.

6.1.2. Host-controlled Mode

In host-controlled mode, a host MCU is connected to the KX1400 using a 4 or 5-wire host interface. Using this interface, the host can send audio data directly to the audio processor, select one of 4096 different phrases to play from an external memory, play tones using the on-chip tone generator, or change the configuration of the KX1400.

6.2. Supported Commands

Table 6.1 lists the commands supported by the KX1400. Commands can be issued from either the host MCU or as part of a phrase processed from external memory. Commands belong to one of two execution types: control and audio. Control commands can be executed at any time, including while an audio command is in the process of execution. Audio commands are executed only after the completion of any pending command (control or other audio command). Refer to Section 8 for detailed information on the KX1400 command set.

Table 6.1. KX1400 Command Summary

COMMAND	OPCODE	LENGTH	TYPE	DESCRIPTION
Reset	0000	8 Bits	Control	Cancels any pending operation and returns the device to its default configuration.
Stop	0001	8 Bits	Control	Halts the processing of any active audio command or phrase.
Set Duration	0010	16 Bits	Control	Specifies the length of time the tone generator plays tones in response to Play Tone commands.
Play Tone	XX11	16 Bits	Audio	Instructs the tone generator to synthesize a tone at the specified frequency.
Mute	0100	8 Bits	Control	Disables the speaker driver.
Un-mute	0101	8 Bits	Control	Enables the speaker driver.
Play Phrase	0110	16 Bits	Audio	Retrieves and processes a phrase from external memory.
Set Volume	1000	8 Bits	Control	Sets the volume level of the output.
Set Outputs	1001	8 Bits	Control	Sets the state of the two general purpose output pins.
Play ADPCM	1010	16 Bits	Audio	Sends 4-bit IMA ADPCM data to the audio processor.
Set Clock	1100	8 Bits	Control	Enables/Disables the clock output (CLKOUT) and selects frequency.
-	1101	8 Bits	Control	Reserved.
Play PCM	1110	16 Bits	Audio	Sends 12-bit PCM data to the audio processor.

6.3. External Memory Interface

The KX1400 includes a SPI™/Microwire™ compatible serial memory interface controller designed to access a user-programmed external serial memory. This memory interface controller implements all of the protocol necessary to address and read numerous third-party EEPROM and Flash serial memory devices. The memory interface supports SPI mode 0 with a fixed clock rate of 4 MHz. Refer to Figure 6.1 and Table 6.2 for detailed timing information.

Figure 6.1. External Memory Interface Timing Diagram

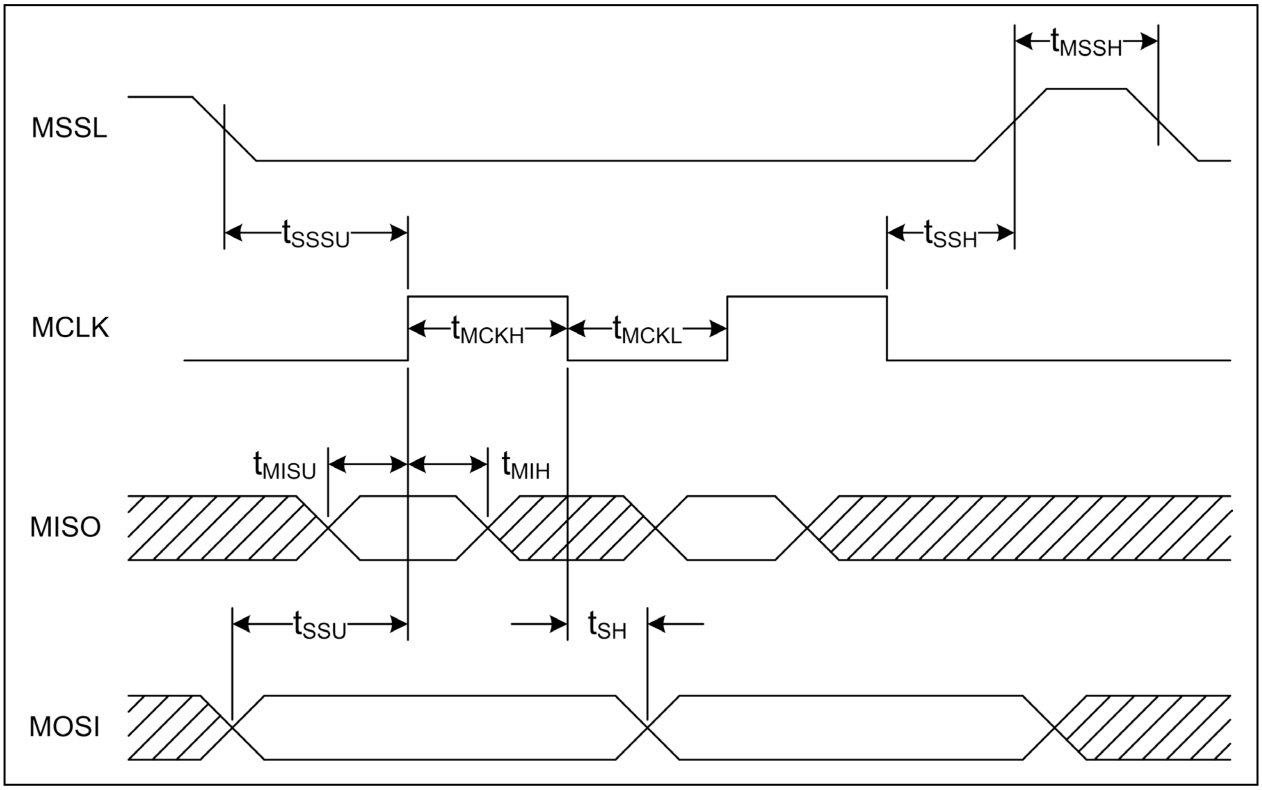


Table 6.2. External Memory Interface Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{SSSU}	Slave Select Setup Time	200		ns
t_{SSH}	Slave Select Hold Time	200		ns
t_{MSSH}	Slave Select High Time	200		ns
t_{MCKH}	MCLK High Time	100		ns
t_{MCKL}	MCLK Low Time	100		ns
t_{MISU}	MISO Valid to MCLK Falling Edge	100		ns
t_{MIH}	MISO Valid Hold Time	0		ns
t_{SSU}	MOSI Valid to MCLK Rising Edge	100		ns
t_{SH}	MOSI Valid Hold Time	100		ns

6.3.1. Memory Size Configuration

The memory interface controller supports the use of serial memories with either 16-bit or 24-bit address spaces. The address size is configured by the state of the MSIZE pin. If MSIZE is set to logic high, the KX1400 will generate 24-bit addresses when accessing the external memory. If MSIZE is set to logic low, 16-bit addresses are generated. The state of the MSIZE pin should remain fixed and not change between device resets.

Table 6.3. Memory Size Configuration

MSIZE State at End of Reset	Address Size Generated by KX1400
Logic High	24-bit address
Logic Low	16-bit address

6.3.2. Audio Phrases

External memory is used to store pre-programmed audio phrases which can later be played by the KX1400. An audio phrase is a sequence of PCM/ADPCM audio samples, tone-generator sequences, and control commands. A phrase is played by sending a single command from the MCU host (or by executing a device reset if configured in stand-alone mode). The specified phrase is retrieved from external memory and its data and commands are streamed to the audio processor at the required data rate. Up to 4096 unique audio phrases can be addressed and retrieved. The length of a phrase is limited only by the space available in the external memory.

6.3.3. Memory Organization

The external memory contains audio phrases and an address table consisting of the locations of the first byte of each phrase stored in memory. The address table is stored at the beginning of the memory starting at address 0. Each address occupies 2 or 3 bytes depending on the state of the MSIZE pin and is stored least-significant-byte (LSB) at the lowest address. Audio phrases are stored sequentially, immediately following the address table, with the first byte of the phrase stored at the lowest address.

For example, with MSIZE = 1 (24-bit addressing), the LSB of the starting address of Phrase 0 is stored starting at 000000h, the LSB of the starting address of Phrase 1 is stored starting at 000003h, and so on. When a Play Phrase command is issued, the KX1400 uses the phrase index field of the command to determine which address to retrieve from the address table. The retrieved address is then used to access the first byte of the phrase.

The phrase is processed by retrieving sequential bytes from the external memory until a Stop command is encountered, marking the end of the phrase. Phrase data is stored little-endian (least significant byte of multi-byte commands stored at the lowest address.) Figure 6.2 illustrates the contents of an external memory that uses 24-bit addressing and contains two phrases.

In stand-alone operation, the first address (lowest address) in the address table is used to retrieve the audio phrase to be played. In the example shown in Figure 6.2, the phrase starting at address 000006h would be played after each device reset.

Figure 6.2. Example External Memory Organization (MSIZE=1)

FFFFFFh	
FFFFFBh	Stop Command
	. More Phrase 1 Commands .
0002FFh	Phrase 1 – First Command
0002FEh	Stop Command
	. More Phrase 0 Commands .
000006h	Phrase 0 – First Command
000005h	00h
	02h
000003h	FFh
	00h
	00h
000000h	06h

6.3.4. Programming External Memory In-System

External Flash and EEPROM memory can be programmed in-system via the KX1400. To access external memory directly, a command is sent via the MCU host interface to configure the KX1400 to operate in pass-thru mode. In pass-thru mode, the MCU host interface pins are mapped directly to the external memory interface. No serial memory access protocol is implemented. The device driving the MCU interface pins must implement the appropriate protocol to access the connected serial memory.

Table 6.4. Pin Mapping in Pass-Thru Mode

MCU INTERFACE	EXTERNAL MEMORY INTERFACE
SCL	MCLK
SDI	MOSI
BUSY	MISO
$\overline{CS}$	MSSL

Pass-thru mode is entered by setting the Pass-thru Option Bit (Bit 5) of the Reset Command. Once entered, the KX1400 remains in pass-thru mode until a device reset occurs. See Section 8.1 for more information on the Reset command.

6.4. Host MCU Interface

The KX1400 provides an interface for transmitting audio data and control commands to the KX1400 from an MCU host. The host MCU interface consists of five signals: three serial data signals output by the MCU and two status signals generated by the KX1400.

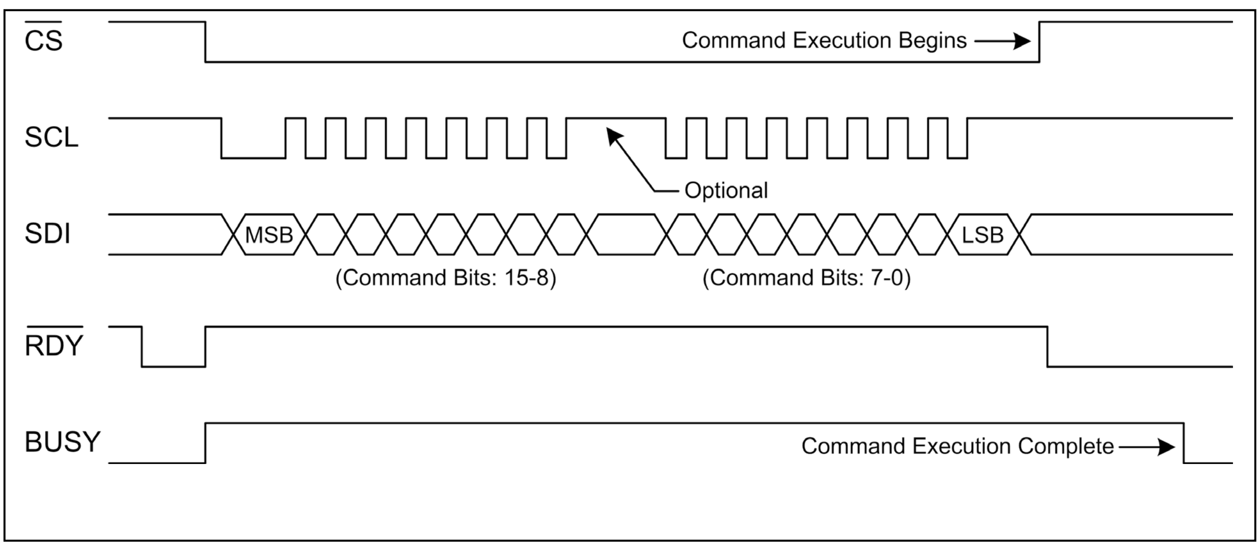
- SCL – Serial Data Clock, output from the MCU
- SDI – Serial Data Input, output from the MCU
- $\overline{\text{CS}}$ – Chip Select (serial interface enable), output from the MCU
- $\overline{\text{RDY}}$ – Ready Status Signal, output from the KX1400
- BUSY – Busy Status Signal, output from the KX1400

In some applications, only one of the status signals ($\overline{\text{RDY}}$ or BUSY) may be necessary, thereby reducing the number of MCU I/O pins required. The three serial data signals are compatible with SPI™ and Microwire™ master controllers and support SPI mode 0 with a maximum clock rate approaching 4 MHz. Refer to Figure 6.4 and Table 6.5 for detailed timing information

6.4.1. Host MCU Interface Operation

When using the host MCU interface to control the KX1400, serial data flows in one direction only, from the MCU to the KX1400. No serial data is returned from the KX1400. Two status signals ($\overline{\text{RDY}}$ and BUSY) indicate the current state of the KX1400. The $\overline{\text{RDY}}$ signal is asserted when the KX1400 is ready to accept the next data word from the host into its two-deep command buffer. BUSY is asserted when the KX1400 has completed execution of all pending commands from its buffer.

Figure 6.3. MCU Host Interface Operation



After $\overline{\text{RDY}}$ is asserted by the KX1400, asserting $\overline{\text{CS}}$ enables an internal shift register to receive data from the host. Data from SDI is clocked into the shift register on each rising edge of the clock signal (SCL). Data is sent most-significant-bit (MSB) first and must be transmitted as a complete 8-bit or 16-bit word. After clocking all 8 or 16 bits into the shift register, a rising edge of $\overline{\text{CS}}$ is required to latch the data into the command buffer and initiate command execution (Figure 6.3). If space remains available in the two-deep command buffer, $\overline{\text{RDY}}$ will immediately be re-asserted and the next command transmission may begin.

Note, if more than 8 or 16 bits are transmitted, only the last 8 or 16 bits transmitted before the rising edge of $\overline{CS}$ will be used (depending on the specific command). Any leading extra bits will be ignored.

Once a command begins shifting in, BUSY is asserted and remains asserted until all pending commands have completed execution. The BUSY signal provides a means for sequencing control-type commands for execution after previously initiated audio commands complete. For example, to schedule a Mute or Set Outputs command to execute at the end of playing a tone or phrase, the MCU must monitor the BUSY signal and transmit the control command only after BUSY is de-asserted. Otherwise, the control command will execute before completion of any current or pending audio commands.

It is possible to operate the host MCU interface without using the $\overline{RDY}$ signal. In such applications, the transmission of each new command is initiated on the de-assertion of BUSY. This configuration requires one less MCU I/O but at the expense of less-relaxed latency requirements provided by the double-buffering of the command buffer.

Figure 6.4 and Table 6.5 provide detailed timing information for the Host MCU Interface signals.

Figure 6.4. Host MCU Interface Timing Diagram

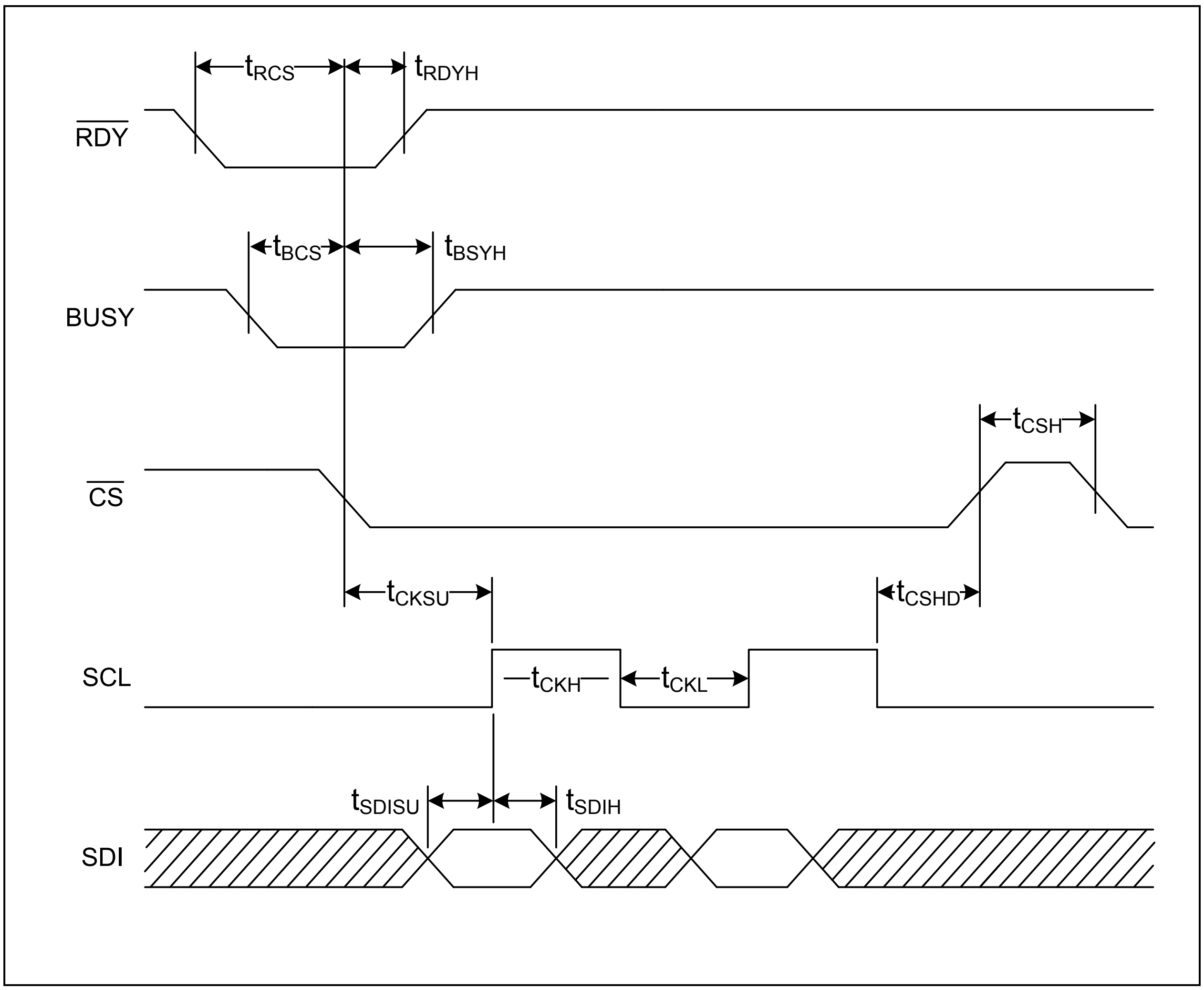


Table 6.5. Host MCU Interface Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{RCS}	$\overline{\text{RDY}}$ to $\overline{\text{CS}}$ Setup Time	0		ns
t_{BCS}	BUSY Falling Edge to $\overline{\text{CS}}$ Setup Time	0		ns
t_{RDYH}	$\overline{\text{CS}}$ to $\overline{\text{RDY}}$ High Time		500	ns
t_{BSYH}	$\overline{\text{CS}}$ to BUSY High Time		625	ns
t_{CKSU}	$\overline{\text{CS}}$ to First SCL Rising Edge Time when not in stand-by state	150		ns
t_{CKSU}	$\overline{\text{CS}}$ to First SCL Rising Edge Time when in stand-by state	500		ns
t_{CKH}	SCL High Time	150		ns
t_{CKL}	SCL Low Time	150		ns
t_{CSH}	$\overline{\text{CS}}$ High Time	150		ns
t_{CSHD}	$\overline{\text{CS}}$ Hold Time	0		ns
t_{SDISU}	SDI Valid to SCL Rising Edge	50		ns
t_{SDIH}	SDI Valid Hold Time	50		ns

6.4.2. Host MCU Command Format

Host MCU commands are either 8 or 16-bits long and consist of a 2 or 4-bit opcode and 4, 12, or 14 bits of data. Some opcodes do not require a data argument but a data field is always required to ensure the entire command word is 8 bits or 16 bits wide. In these cases, the value of the data field is ignored, and therefore may be set to any convenient value. Commands are sent to the MCU interface by transmitting the command into the shift register most-significant-bit (MSB) first. The opcode is the 2 or 4 least-significant bits (LSBs) of the command word and is therefore sent last. Figure 6.5 illustrates the format of a typical 16-bit command.

Figure 6.5. Example of a 16-bit Command

First Bit Transmitted | **Last Bit Transmitted**

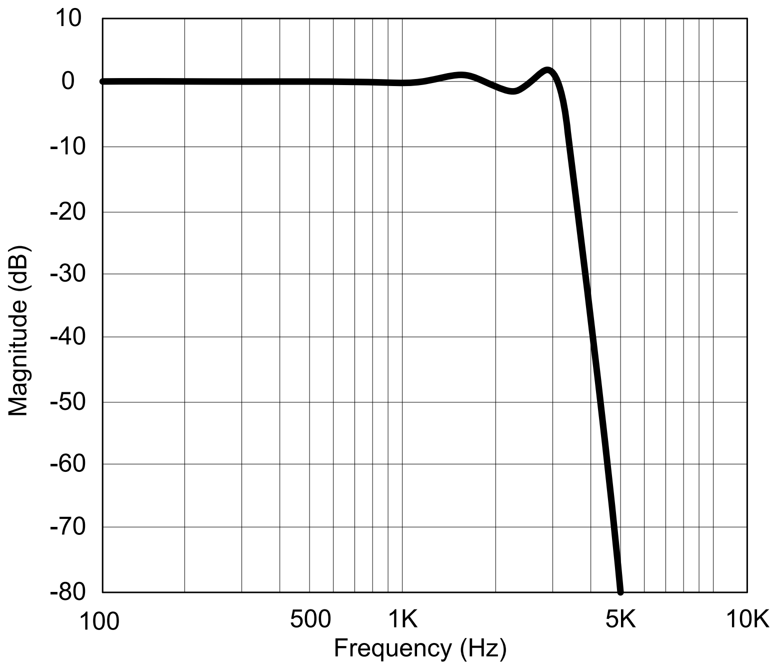
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Data												Opcode			

6.5. Digital Audio Processor

The on-chip Digital Audio Processor incorporates an audio data decoder and 12-bit delta-sigma modulator. It supports audio data sampled at 8 kHz and encoded in the IMA ADPCM or 12-bit PCM (2's-complement, uncompressed) formats. Oversampling and second-order noise shaping techniques are employed to ensure quantization noise generated by the delta-sigma modulator is suppressed within the audio band.

The output signal is an enhanced, 256 kHz pulse-width-modulation representation of the audio signal. The switching frequency of this signal is well beyond the audio range and therefore requires only minimal low-pass filtering. Typically, the response characteristics of the external speaker are sufficient, eliminating the need for additional filtering.

Figure 6.6. Audio Processor Frequency Characteristics



6.6. Volume Control

The Digital Audio Processor includes a volume control function. Volume control is performed by digitally adjusting the amplitude of the signal level before sending to the class-D amplifier stage. The amplitude can be varied from 0 to 100 percent in 16 equal linear steps.

The volume is adjusted by sending the Set Volume command via the MCU host interface or as part of a phrase processed from external memory. Refer to Section 8.8 for detailed information on the use of the Set Volume command. Note: a volume level of zero does not mute the output (disable the speaker driver). It only attenuates the audible components of the output signal. Use the Mute and Un-mute commands to disable/enable the output signal (see Section 6.8).

6.7. Tone Generator

The on-chip tone generator synthesizes audio data in the form of a single sine wave of a specified frequency for a specified period of time. Tones can easily be sequenced together to play musical melodies or generate sound effects. Sounds created by storing and sending commands to the tone generator can produce significant savings in data storage requirements over storing and playing recorded PCM or ADPCM audio data.

6.7.1. Tone Frequency

Tones are created by sending the Play Tone command via the MCU host interface or as part of a phrase processed from external memory. The Play Tone command includes a Frequency Index which specifies the frequency to be generated in Hertz using the following formula:

$$Frequency = \frac{Index}{4.096} Hz$$

The Frequency Index takes a value from 0 to 16383. Therefore, frequencies can be generated in the range of 0.24414 Hz to 3.9997 KHz. A Frequency Index of 0 causes the KX1400 IC to repeat the previous tone but mute the output for the duration of the tone. This allows the IC to generate a controlled period of silence. The outputs are automatically un-muted when the next audio command is processed.

6.7.2. Tone Duration

The length of time each tone is played is determined by the currently configured duration value. The duration value represents time in milliseconds and may be configured with a value from 0 to 4095. Therefore, tone durations may range from 1 millisecond to 4.095 seconds in 1 millisecond increments. Durations longer than 4.095 seconds can be created by repeating the Play Tone command in order to extend the playing of a tone.

At the end of the duration period, any pending audio command will execute. Otherwise, the tone generator will halt and speaker driver output will return to a DC average (no tone). A value of 0 corresponds to an infinite duration (tones will play until a Reset, Stop or new audio command, such as another Play Tone command, is issued).

After reset, the default duration value is 0 (infinite duration). The duration value is configured by sending a Set Duration command via the MCU host interface or as part of a phrase processed from external memory. Once configured, the duration value remains in effect for all subsequent Play Tone commands or until a new duration is set. It is possible to issue a Set Duration command before each new Play Tone command, thereby allowing each tone in a sequence to have a different duration.

6.8. Speaker Driver

The KX1400 includes a speaker driver suitable for driving an 8-ohm (or greater) speaker directly. The speaker driver incorporates a class-D amplifier stage with differential outputs connected to the SPO+ and SPO- pins.

A mute feature is provided to save power when not producing sound and to prevent possible speaker pops and clicks during device power-on/off. The mute feature disconnects the internal speaker driver amplifiers from the SPO+ and SPO- output pins and terminates them to ground.

The mute feature is controlled by sending Mute and Un-mute commands via the MCU host interface or as part of a phrase processed from external memory. A stepping algorithm is employed which gradually ramps the speaker output up/down between the currently configured volume level and the zero output level. The output is ramped at a rate of one volume level increment every 1 ms. During power-up or after a device reset, the speaker driver is muted and the volume level set to full volume. It is recommended the speaker driver be muted before powering down or resetting the device if possible. Refer to Section 8 for more information regarding the Mute and Un-mute commands.

6.9. On-chip Oscillator

The KX1400 includes a factory calibrated, internal 8.2 MHz oscillator used as the system time base. No external components are necessary for calibration or operation. Electrical specifications for the precision internal oscillator are given in Table 6.6 Specifications are for T_A = -20°C to +70°C, VDD = 2.7V to 5.5V unless otherwise specified.

Table 6.6. Internal Oscillator Electrical Specifications

SYMBOL	PARAMETER	CONDITION	Min	Typ	Max	Units
fosc	Internal Oscillator Frequency	VDD = 3.3V, T = 25°C	8.07	8.192	8.32	MHz
Δf_{OSC}	Internal Oscillator Frequency Variation	2.7V ≤ VDD ≤ 3.6V	-1		+1	%
		2.7V ≤ VDD ≤ 5.5V	-1		+3	%

6.10. General Purpose Clock Output

The KX1400 provides a Clock Output feature with the ability to divide the frequency of the internal precision oscillator and route this signal to the CLKOUT pin. This signal may be used as a time base by other components in the system. (Note: it is not required to use this signal to synchronize the MCU with the KX1400. The MCU interface may operate asynchronously to the internal system clock used by the audio processor, including while streaming audio data to the KX1400 from a host MCU.)

The divisor used to divide the 8.2 MHz internal system clock before the signal is output on the CLKOUT pin is configured by sending a Set Clock command via the MCU host interface or as part of a phrase processed from external memory. Table 6.7 shows the possible Clock Divisor values and corresponding frequencies output on the CLKOUT pin.

Table 6.7. Clock Divisor and Output Frequencies

CLOCK DIVISOR	8.2 MHz INTERNAL CLOCK DIVIDED BY:	CLKOUT FREQUENCY
0	1	8.2 MHz
1	2	4.1 MHz
2	4	2.05 MHz
3	8	1.025 MHz

The Clock Output feature is enabled by default after a device reset with the Clock Divisor set to divide by 8 (1.025 MHz CLKOUT signal). It may be disabled with the CLKOUT pin forced to the desired steady state level using the Set Clock command. Refer to Section 8.12 for detailed information on the use of the Set Clock command. Internal hardware synchronizes execution of the Set Clock command to ensure minimum pulse width specifications are maintained when changing the Clock Divisor or disabling/enabling the Clock Output feature.

6.11. General Purpose Digital Outputs

The KX1400 provides two general purpose digital outputs mapped to the GPO1 and GPO2 pins. The state of these pins is controlled by issuing the Set Outputs command via the host MCU interface or as part of a phrase processed from external memory. The output drivers for these pins may be configured as open-drain or push-pull. Refer to Section 8.9 for detailed information on use of the Set Outputs command. After device reset, all outputs are set to logic level low with push-pull drive characteristics.

6.12. Stand-by Mode

A low-power Stand-by mode is available via an option of the Stop command. In Stand-by mode, all audio and command processing is halted, the speaker driver is disabled and the internal oscillator is stopped. Power consumption is reduced to about 1 µA (excluding load current sourced by the GPO1/2 outputs).

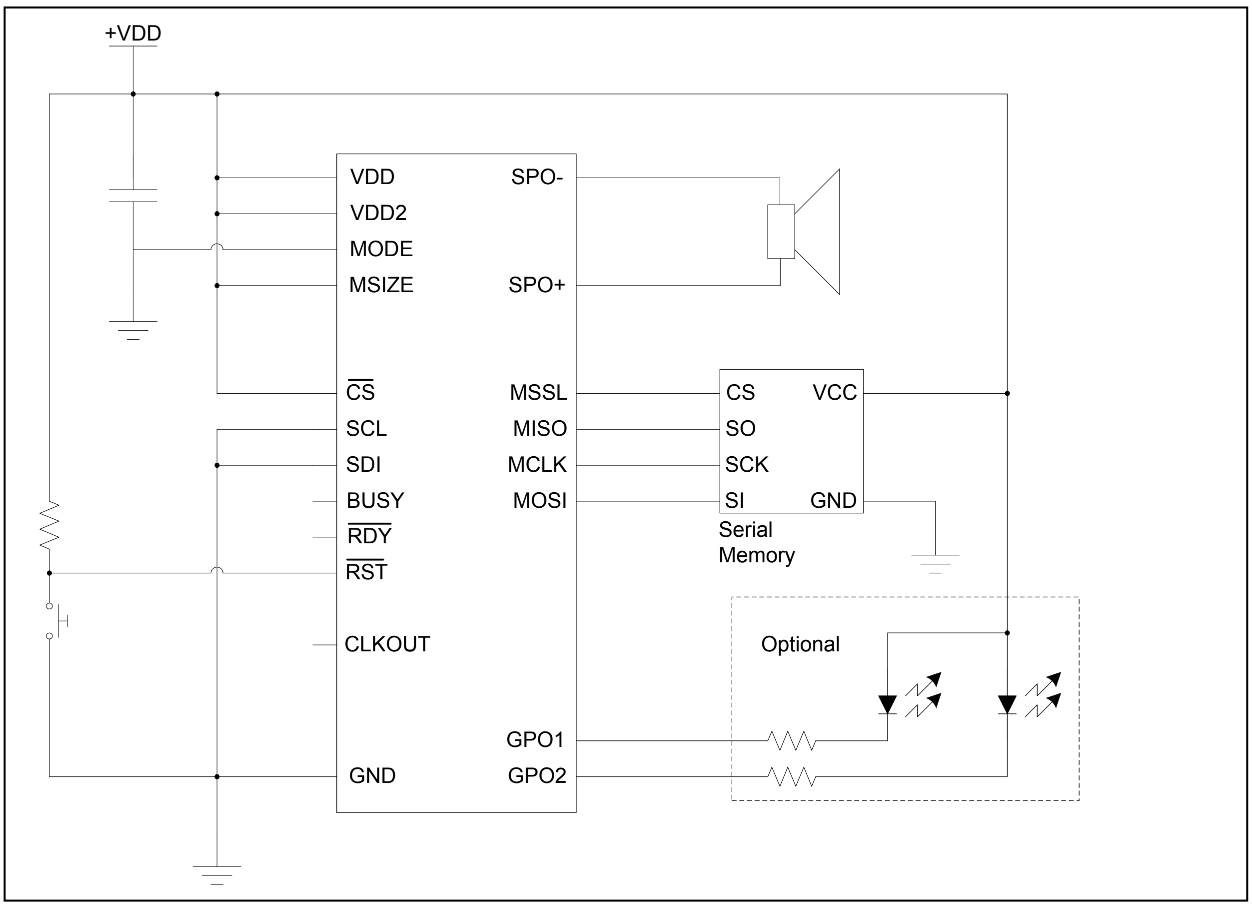
Stand-by mode is entered by setting the Stand-by Option bit when issuing the Stop command via the MCU host interface or as part of a phrase processed from external memory. Stand-by Mode is exited by performing a device reset or on the next falling edge of the $\overline{CS}$ signal. If using the $\overline{CS}$ signal to exit Stand-by mode, the first rising edge of the SCL clock signal must be delayed at least 500 ns after the $\overline{CS}$ signal is asserted when using the Host MCU interface. Refer to Section 8.2 for detailed information on the use of the Stop command and the Stand-by mode option.

7. EXAMPLE APPLICATION CIRCUITS

7.1. Stand-Alone Operation

Following is an example circuit with the KX1400 operating in stand-alone mode and optional LEDs connected to general purpose outputs. The LEDs are controlled with Set Outputs commands embedded in audio data played from the attached serial memory. A single audio phrase is played each time the push-button switch connected to $\overline{RST}$ pin is pushed/released.

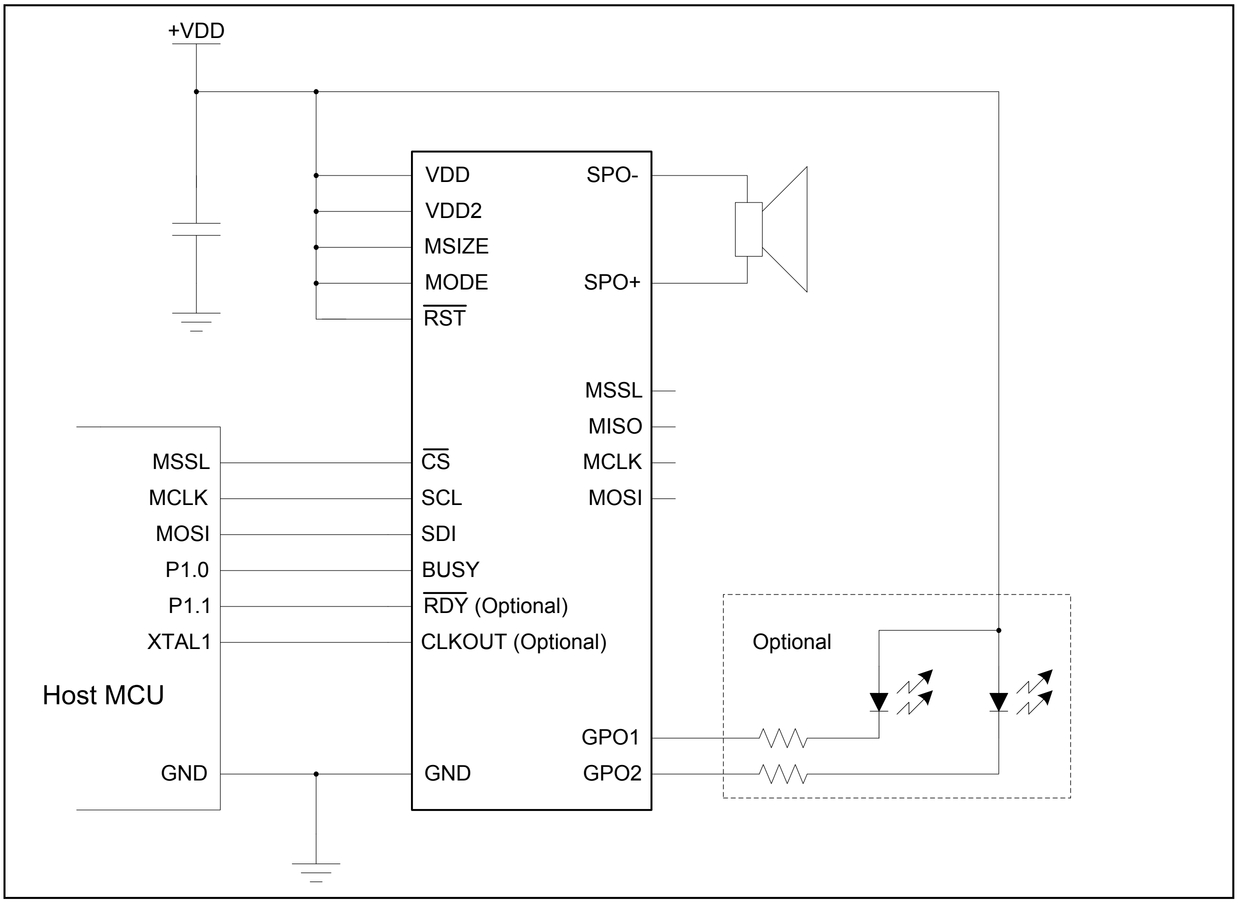
Figure 7.1. KX1400 in Stand-alone Operation



7.2. Host Controlled without External Memory

The following example circuit shows the KX1400 in host-controlled operation with audio data stored in the MCU's data memory. LEDs are controlled with Set Outputs commands sent from the MCU. The CLKOUT signal from the KX1400 is used as the MCU's system clock (optional).

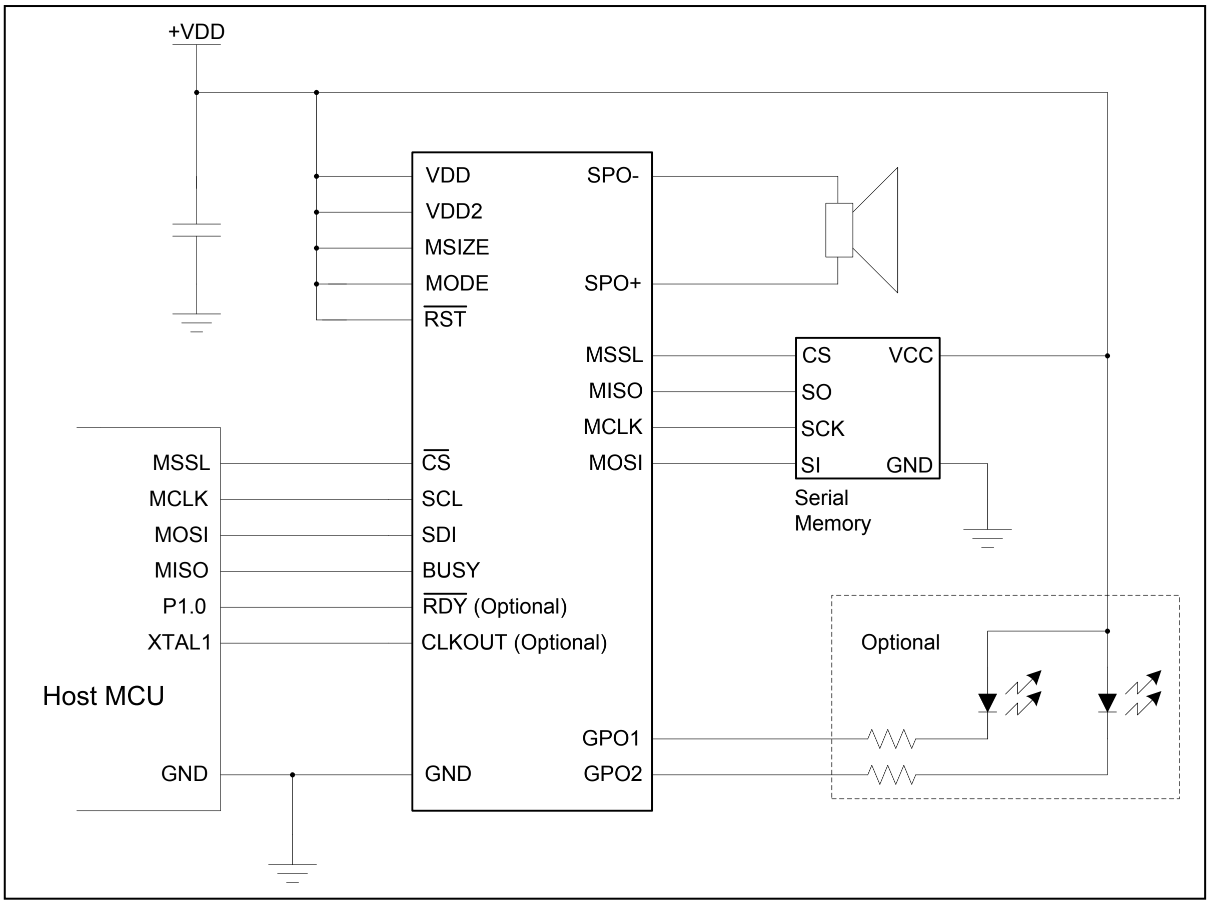
Figure 7.2. KX1400 in Host-Controlled System



7.3. Host Controlled with External Memory

The example circuit in Figure 7.3 shows the KX1400 in host-controlled operation with audio data stored in external serial memory. Commands are sent from the MCU to play audio phrases from the external memory. The BUSY pin is connected to the host MCU's MISO signal to allow programming the external memory in-system via the MCU. The LEDs are controlled with commands sent from the MCU and the CLKOUT signal from the KX1400 is used as the MCU's system clock (optional).

Figure 7.3. KX1400 in Host-controlled Operation with External Memory



8. COMMAND SET

8.1. Reset

Encoding:

Bits 7-6	Bit 5	Bit 4	Bits 3-0
Unused	SPI Pass Thru	Disable Mem I/F	0000

Description: The Reset command cancels any pending operation, immediately disables output to the speaker driver, and resets the tone-duration setting to zero. The CLKOUT and GPO states are not affected. The $\overline{RDY}$ pin is asserted at the end of the reset operation. If the Reset command is encountered in a phrase played from external memory during stand-alone mode, the phrase address counter is reset causing the phrase to be repeated continuously.

Type: Control

Options: Bit 4: Disable Memory I/F
Setting the Disable Memory Interface option to logic one disables the external memory interface and tri-states the following pins: MOSI, MISO, MCLK, and MSSL.

Bit 5: SPI Pass-Thru Mode
Setting the SPI Pass-Thru option to logic one connects the MCU host interface pins directly to the external memory interface, allowing the external memory to be accessed in system via the MCU host interface. Note: In SPI Pass-thru mode, the GPO1 pin is connected to the MISO pin of the external memory interface. Once entered, the KX1400 remains in Pass-thru mode until a device reset occurs (a power-off/power-on sequence or asserting and releasing the $\overline{RST}$ pin).

Data: None

Length: 8 Bits

8.2. Stop

Encoding:

Bits 7-5	Bit 4	Bits 3-0
Unused	Stand-by	0001

Description: When issued from the host MCU, the Stop command immediately terminates the execution of any audio command. The speaker outputs are not automatically muted.

The Stop command is also used to mark the end of a phrase stored in external memory. Once processing of a phrase from external memory begins, data and commands are continually retrieved and processed until the Stop command is encountered. The last audio command (e.g. Play Tone) issued before the Stop command in a phrase is not immediately terminated but allowed to run to completion.

Note: The KX1400 will ignore all incoming commands while executing a Play ADPCM command from external memory, including the Stop command. To stop a Play ADPCM command from external memory, a hardware reset must be performed.

Type: Control

Options: Bit 4: Stand-by
Setting the Stand-by option to logic one executes a mute operation and then puts the KX1400 into its low-power stand-by state. The stand-by state is exited at the next assertion of the $\overline{CS}$ signal (i.e. at the beginning of the next MCU interface transmission) or after a device reset.

Data: None

Length: 8 Bits

8.3. Set Duration

Encoding:

Bits 15-4	Bits 3-0
Duration	0010

Description: The Set Duration command is used to specify the length of time the tone generator plays tones in response to Play Tone commands. At the end of the duration period, any pending audio command will execute. Otherwise, the tone generator will halt and the speaker driver output will return to a DC level (go silent).

After reset, the default duration value is 000h which corresponds to an infinite duration (tones will play until a Reset, Stop or new audio command is issued). Once configured using the Set Duration command, the duration period remains in effect for all subsequent Play Tone commands or until a new duration is set.

Type: Control

Options: None

Data: Bits 15-4: Duration
The length of time in milliseconds the tone generator plays tones in response to Play Tone commands. A value of 000h corresponds to an infinite duration (tones will play until a Reset, Stop or new audio command is issued).

Length: 16 Bits

8.4. Play Tone

Encoding:

Bits 15-4	Bits 1-0
Frequency Index	11

Description: The Play Tone command instructs the tone generator to synthesize the appropriate audio data and send it to the audio processor to create a tone at the specified frequency. The length of time the tone is played depends on the current duration setting. (See the Set Duration command for more information.)

Type: Audio

Options: None

Data: Bits 15-4: Frequency Index
The Frequency Index specifies the frequency generated in Hertz using the following formula: Frequency = (Index / 4.096) Hz. A Frequency Index of 000h repeats the previous tone but mutes during the duration of the tone. This allows the generation of timed periods of silence.

Length: 16 Bits

8.5. Mute

Encoding:

Bits 7-4	Bits 3-0
Unused	0100

Description: The Mute command disables the speaker driver. The SPO+ and SPO- pins are terminated to ground after speaker output is gradually ramped down at a rate of one volume level increment per millisecond (from the currently configured volume level to 0). Note the Mute command does not terminate the processing of any current or future audio command, it only silences the output.

Type: Control

Options: None

Data: None

Length: 8 Bits

8.6. Un-mute

Encoding:

Bits 7-4	Bits 3-0
Unused	0101

Description: The Un-mute command enables the speaker output. The speaker output is gradually ramped up at a rate of one volume level increment per millisecond (from 0 to the currently configured volume level).

Type: Control

Options: None

Data: None

Length: 8 Bits

8.7. Play Phrase

Encoding:

Bits 15-4	Bits 3-0
Phrase Index	0110

Description: The Play Phrase command instructs the KX1400 to retrieve and process a specified phrase from external memory. A maximum of 4096 unique phrases is supported.

Type: Audio

Options: None

Data: Bits 15-8: Phrase Index
The Phrase Index is an ordinal identifier specifying one of a possible 4096 unique phrases to be retrieved and processed from external memory. See Section 6.3.3 for more information on external memory organization and how phrase data is stored and accessed.

This command should not be used within a phrase to be processed from external memory. Issuing this command from external memory will effectively deadlock the device until a device reset takes place.

Length: 16 Bits

8.8. Set Volume

Encoding:

Bits 7-4	Bits 3-0
Volume Level	1000

Description: The Set Volume command configures the speaker driver to one of 16 output levels. A value of 1111 corresponds to the maximum output level and 0000 the lowest. Note: a volume level of zero does not mute the output (disable the speaker driver). It only silences the audible components of the output signal.

Type: Control

Options: None

Data: Bits 7-4: Volume Level
Specifies one of 16 speaker output levels with 1111 corresponding to the maximum output level and 0000 the lowest.

Length: 8 Bits

8.9. Set Outputs

Encoding:

Bits 7-5	Bit 4	Bits 3-0
Outputs Configuration	0 (Reserved)	1001

Description: The Set Outputs command sets the state of the two general purpose output pins. The output drivers for the general purpose output pins may be configured as open-drain or push-pull. The default configuration after a device reset is both outputs set to logic level low with push-pull drive characteristics.

Type: Control

Options: None

Data: Bit 4: Reserved
This bit is reserved and should always be set to logic zero. Behavior when setting this bit to logic one is undefined.

Bits 7-5: Outputs Configuration
Specifies the output driver characteristics and levels for the two general purpose output pins.

Bits 7-5	Outputs State
X00	X = 0: output drivers are push-pull, X= 1: output drivers are open-drain
L01	Sets GPO1 output level to L (0 = logic low, 1 = logic high)
L10	Sets GPO2 output level to L (0 = logic low, 1 = logic high)
L11	Sets GPO1 and GPO2 output levels to L (0 = logic low, 1 = logic high)

Length: 8 Bits

8.10. Play ADPCM (From MCU)

Encoding:

Bits 15-12	Bits 11-8	Bits 7-5	Bit 4	Bits 3-0
ADPCM Sample 2	ADPCM Sample 1	Unused	ADPCM Reset	1010

Description: When issued from the host MCU interface, the Play ADPCM command sends two 4-bit, 8 kHz IMA ADPCM audio samples to the KX1400 audio processor. This command can be repeated with new data to stream a continuous ADPCM audio sequence to the KX1400 in real time. If a new Play ADPCM or other audio command is not issued within two sample periods (250 μs) of the previous command, the speaker output level will be maintained at its last level, in effect silencing the output.

Type: Audio

Options: Bit 4: ADPCM Reset
Setting this bit to a logic one resets the ADPCM decoder state. The ADPCM decoder must be reset at the beginning of each new ADPCM sequence. Therefore, this bit should be set when the command is issued with the first two samples in the sequence and then cleared in all subsequent commands until a new sequence is started.

Data: Bits 11-8: ADPCM Sample 1
This is a 4-bit, 8 kHz IMA ADPCM audio sample. Sample 1 is processed before Sample 2.

Bits 15-12: ADPCM Sample 2

This is a 4-bit, 8 kHz IMA ADPCM audio sample. Sample 2 is processed after Sample 1.

Length: 16 Bits

8.11. Play ADPCM (From External Memory)

Encoding:

Bits 31-8	Bits 7-5	Bit 4	Bits 3-0
Number of Bytes	Unused	ADPCM Reset	1010

Description: When used within a phrase to be processed from external memory, the Play ADPCM command instructs the KX1400 to retrieve a specified number of IMA ADPCM audio samples from external memory to be decoded and sent to the Digital Audio Processor at the appropriate sample rate. The ADPCM sample data is expected to be organized in external memory two samples per byte. The sample stored in the low-order nibble (least-significant 4 bits) is played first.

Note: The KX1400 will ignore all incoming commands while executing a Play ADPCM command from external memory, including the Stop command. To abort a Play ADPCM command from external memory, a hardware reset must be performed.

Type: Audio

Options: Bit 4: ADPCM Reset
Setting this bit to a logic one resets the ADPCM decoder state. The ADPCM decoder must be reset at the beginning of each new ADPCM sequence.

Data: Bits 31-8: Number of Bytes
When using an external memory with 24-bit addressing (MSIZE =1) bits 31-8 represent the number of sequential bytes that will be retrieved and processed as 4-bit, 8 kHz IMA ADPCM data. ADPCM data is packed two samples per byte; therefore, this number is calculated as the number of ADPCM samples divided by two. (The number of ADPCM samples must be even.)

If the external memory uses 16-bit addressing (MSIZE = 0) bits 23-8 are used for the 16-bit byte count and the next following byte of memory (bits 31-24) is the first byte of ADPCM data.

Length: 24 or 32 Bits

8.12. Set Clock

Encoding:

Bit 7	Bit 6	Bits 5-4	Bits 3-0
Clock-out Disable	Clock-out Stop State	Clock Divisor	1100

Description: The Set Clock command is used to enable/disable the Clock Output feature and to specify the frequency of the clock-out signal.

Type: Control

Options: Bit 6: Clock-out Stop State

The Clock-out Stop State option defines the output level of the CLKOUT pin when the Clock-out signal is disabled. Setting this bit to logic one sets the CLKOUT output to a logic level high state. Setting it to logic zero sets the CLKOUT output to logic level low.

Note: this option also allows the use of the CLKOUT pin as a general purpose output when not using the clock-out feature. The CLKOUT pin may be toggled by toggling the Clock-out Stop State bit while Clock-out Disable is set. The CLKOUT pin's drive characteristic is always push-pull.

Bit 7: Clock-out Disable
Setting the Clock-out Disable bit to logic one disables the clock-out feature and sets the CLKOUT pin to the logic level defined by the Clock-out Stop State option. Setting it to logic zero enables the Clock Output feature. The Clock Output feature is enabled by default after a device reset (Clock-out Disable = 0).

Data: Bits 5-4: Clock Divisor
Specifies the divisor used to divide the 8.2 MHz system clock before the signal is output on the CLKOUT pin. The Clock Divisor is set to divide by 8 (1.024 MHz CLKOUT signal) by default after a device reset.

CLOCK DIVISOR (Bits 5-4)	8.2 MHz INTERNAL CLOCK DIVIDED BY:	CLKOUT FREQUENCY
00	1	8.2 MHz
01	2	4.1 MHz
10	4	2.05 MHz
11	8	1.024 MHz

Length: 8 Bits

8.13. Play PCM

Encoding:

Bits 15-4	Bits 3-0
PCM Data	1110

Description: The Play PCM command is used to send uncompressed 12-bit, two's complement, PCM audio data directly to the KX1400 audio processor in real time. If a new Play PCM or other audio command is not issued within one sample period (125 µS) of the previous Play PCM command, the audio processor will repeat the previous PCM audio data.

Type: Audio

Options: None

Data: Bits 15-4: PCM Data
Uncompressed 12-bit, two's-complement, PCM audio data sampled at 8 kHz.

Length: 16 Bits

Ordering Part Number	Package/Case	Operating Temp.	Packaging
KX1400EW	SOIC-20 300mil	-40°C to 85°C	Tube
KX1400EG	QFN-24 4x4mm	-40°C to 85°C	Tape

Contact Information

Keterex, Inc.

7320 N. Mo Pac Expressway

Suite 201

Austin, Texas 78731

Tel: 512-346-8800

www.keterex.com

Email: support@keterex.com